

## In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1           1.     (Currently Amended) A circuit for interfacing between a  
2 first component operating at a first clock rate and a second  
3 component operating at a second clock rate wherein said second  
4 clock rate is higher than said first clock rate, said circuit  
5 comprising:

6           a first buffer coupled to said first component, said first  
7 buffer receiving and storing data received from said first  
8 component at said first clock rate;

9           a second buffer coupled to said second component, said second  
10 buffer supplying data recalled therefrom to said second component  
11 at said second clock rate;

12          a copy/access controller connected to said first buffer, said  
13 second buffer, and said second component, said copy/access  
14 controller including

15           a counter operable to count each time data is stored in  
16 said first buffer,

17           a comparator having a first input receiving said count of  
18 said counter and a second input receiving a buffer size signal  
19 indicative of a size of said first buffer, said comparator and  
20 operable when said count equals said buffer size to generate a  
21 load signal

22           to copy data from said first buffer to said second  
23 buffer ~~when said first buffer is substantially full,~~ and  
24 ~~further operable~~

25           to prompt said second component to access said  
26 second buffer ~~when said data is copied from said first~~  
27 ~~buffer.~~

1           2.    (Original) The circuit as set forth in Claim 1, wherein  
2 both said first buffer and said second buffer are random-access  
3 memories.

1           3.    (Original) The circuit as set forth in Claim 1, wherein  
2 both said first buffer and said second buffer are shift registers.

1           4.    (Original) The circuit as set forth in Claim 1, wherein  
2 said circuit is integrated onto a semiconductor die with one of  
3 said first component or said second component.